

Okmetic's SOI wafers enable smaller die size and improved device performance

BSOI

Silicon-On-Insulator wafer manufactured by bonding two silicon wafers together with an insulating oxide between

- Typically devices are built on the active layer. Oxide enables complete isolation of devices from the substrate in semiconductor applications. Typical uses for the buried oxide in MEMS applications are forming effective etch-stop, and acting also as a sacrificial layer for releasing MEMS structures. Handle wafer is supporting the structure but it can also be utilized in sealing the structure or as part of device.
- SOI layer thickness up to $> 200 \mu\text{m}$, standard tolerance $\pm 0.3 \mu\text{m}$. Handle wafer thickness $300\text{-}950 \mu\text{m}$, back surface polished or etched. Buried oxide thermally grown SiO_2 .

E-SOI

An enhanced SOI wafer with a new level of layer thickness uniformity and unprecedented properties

- An ideal platform for demanding applications such as HV BCD devices, silicon photonics and high-precision silicon-based MEMS sensors.
- Device layer thickness freely adjustable between $1.0 \mu\text{m}$ and $>100 \mu\text{m}$ and the thickness tolerance independent of target thickness as low as $\pm 0.1 \mu\text{m}$.
- Buried oxide thickness freely adjustable between $0.5 \mu\text{m}$ and $3 \mu\text{m}$.

C-SOI

A bonded SOI wafer with built-in sealed cavities on the handle wafer or on the buried oxide

- Application areas include e.g. pressure sensors, silicon microphones and fluidic components, inertial sensors, IC and MEMS process integration.
- As the patterning is etched before bonding, C-SOI enables complex and developed structures that standard BSOI wafers do not allow.
- The process enables extremely thin membranes and integrated backside packaging and hermetic sealing.

