# OKNETIC



## LITHOGARPHY

# OKMETIC BONDED SOI WAFERS ENABLE IMPROVED DEVICE DESIGNS

BSOI

Fully customizable with starting materials from in-house crystal growth and wafering.

# 0.3 - 501

Improved device layer thickness tolerance  $\pm 0.3 \ \mu m$ .

## **E-SOI®**

Highly uniform wafers with device layer thickness tolerance  $\pm 0.1 \ \mu m$  independent of layer thickness.

## C-SOI®

Wafers with pre-etched cavities. Fully in-house C-SOI® process flow from silicon crystal growth to cavity patterning and SOI wafer manufacturing.

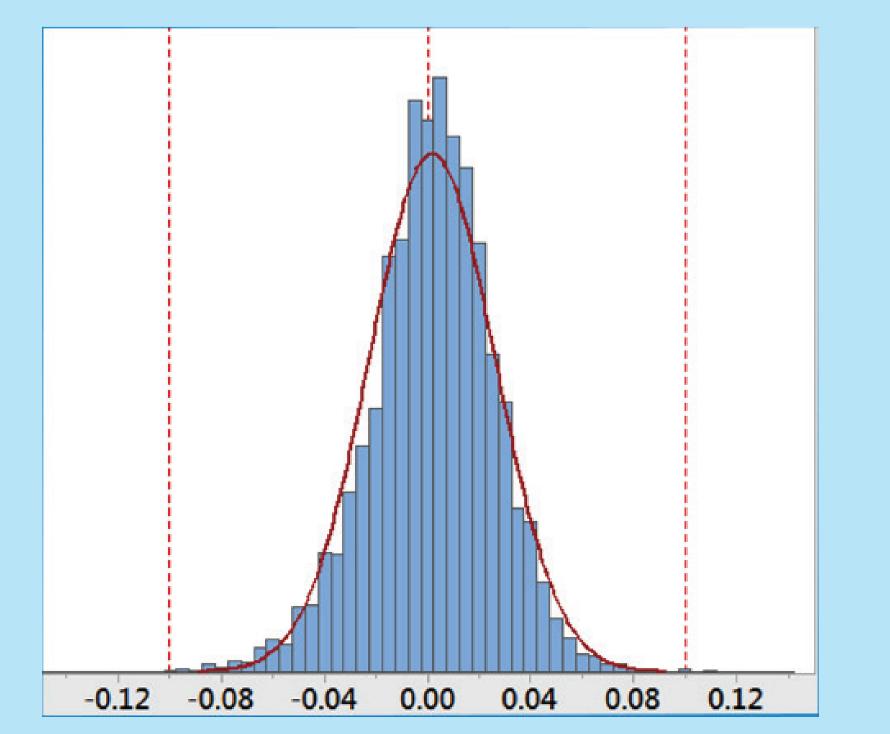
# L-SOI

Low resistivity SOI device layers.

# EC-SOI

Combination of highly uniform E-SOI® wafer with cavity structures of C-SOI® wafer.

#### Device layer thickness capability of E-SOI® wafers



## **TYPICAL SOI SPECIFICATIONS**

### RESISTIVITY

From < 0.001 to > 7,000 Ohm-cm

## **DEVICE LAYER THICKNESS**

From 1  $\mu$ m to > 200  $\mu$ m

Tolerance ±0.5 μm (standard BSOI), ±0.3 μm (0.3 SOI), ±0.1 μm (E-SOI®), ±0.7 μm (C-SOI®)

Deviation from target thickness (µm)

#### HANDLE WAFER THICKNESS

From 300 µm to 950 µm, typically 725 µm in 200mm wafer and 380 µm in 150mm

Back surface polished or etched

### **BURIED OXIDE**

Type: thermal oxide, thickness: from 300 nm to 4  $\mu$ m, typically between 0.5  $\mu$ m and 2  $\mu$ m

