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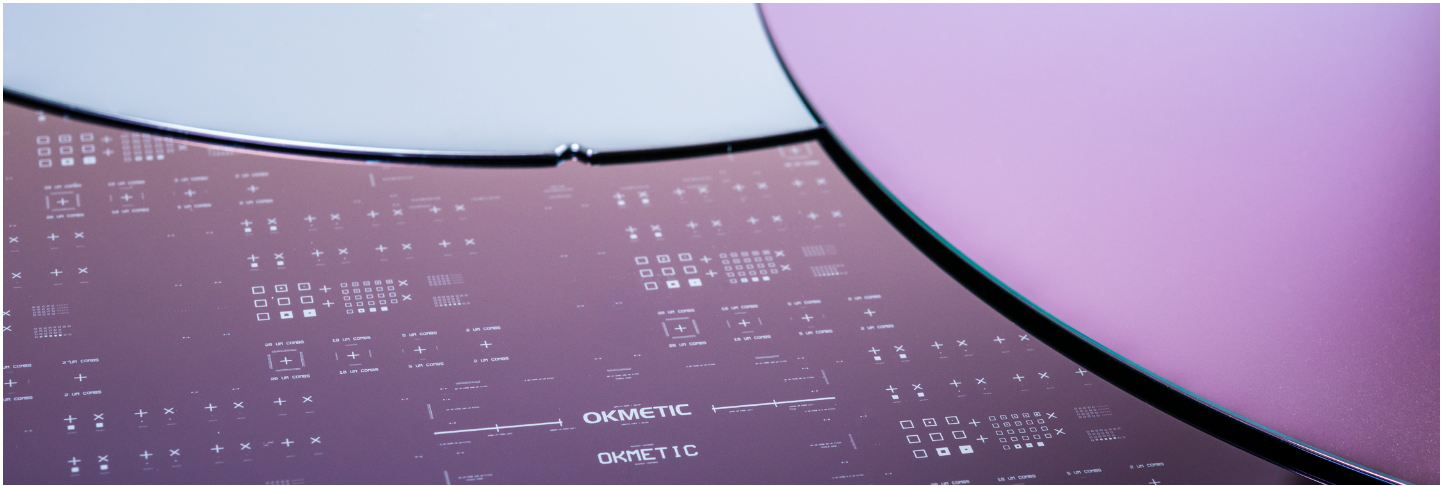


BONDED SOI WAFERS ADD DESIGN FREEDOM AND PERFORMANCE

Bonded SOI and E-SOI® Wafers

- 150-200 mm wafers with fully customizable device handle and BOX layer. Wide selection of dopants, orientations and resistivities for device and handle layer.
- BOX layer is an efficient etch-stop, electric insulator or sacrificial layer.
- E-SOI® wafer with ±0.1 µm device layer thickness variation for higher-precision devices.
- Bonded SOI wafers in volume production since 2001.

Application Areas

Good fit for pressure and inertial sensors, microfluidic devices, MOEMS, flow sensors, silicon speakers, silicon photonics, silicon timing devices and high-precision silicon-based MEMS.

Key Benefits

Cost Efficiency: Simplifies processing and reduces chip size, lowering manufacturing costs and improving yield and reliability.

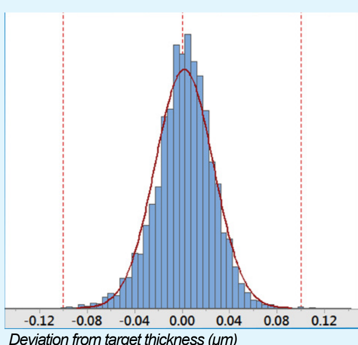
Miniaturization and Integration: Enables compact, multi-functional MEMS devices with high precision and integration on a single wafer.

High Precision: Offers precise control over device layer thickness (±0.1 µm for E-SOI®), ensuring accurate, high-performance devices.

Mechanical Robustness: Withstands environmental stresses like temperature fluctuations, ensuring long-term reliability.

Low Power Consumption: The BOX layer minimizes parasitic capacitance and leakage currents, reducing power consumption, ideal for battery-powered systems.

Device layer thickness capability of E-SOI® wafers



Typical SOI Wafer Specifications

RESISTIVITY

Between <0.001 and >7,000 Ohm-cm

DEVICE LAYER THICKNESS

From 1 µm to > 200 µm
Tolerance ±0.5 µm (standard BSOI), ±0.1 µm (200 mm E-SOI®), ±0.5 µm or lower (C-SOI®)

HANDLE WAFER THICKNESS

300 µm to 950 µm (±3-5 µm)
Back surface polished or etched

BURIED OXIDE

Type: thermal oxide, thickness: 0.3 µm to >5 µm

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