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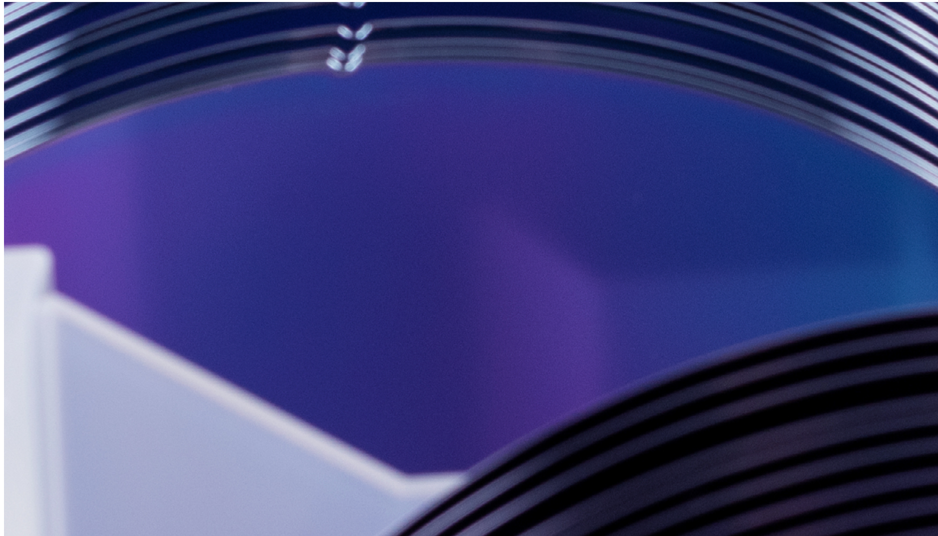


SILICON AND BONDED SOI WAFERS OPTIMIZED FOR POWER DEVICES

Discrete Power Device Wafers

Wafers with customizable resistivity from <0.001 to >1,150 Ohm-cm, controlled resistivity spread, optimized Oi concentration, and low defect density. Suitable for NPT/FS and PT IGBT, power MOSFETs, HV diodes, FRDs, SBDs, thyristors, and other bipolar devices.

Low COP Wafers (Si and SOI)

Wafers with minimal amount of >0.12 µm near-surface defects and optimized GOI performance. Zero COP Bonded SOI available through annealing. Designed for NPT/FS and advanced IGBT applications, as well as power management devices.

Power Management SOI Wafers

Bonded SOI wafers with down to <0.001 Ohm-cm resistivity, tightly controlled resistivity variation, optimized Oi concentration, and low defect density. Suitable for gate drivers, battery and power management ICs, intelligent power modules, and smart power devices using advanced BCD or BiCMOS processes.

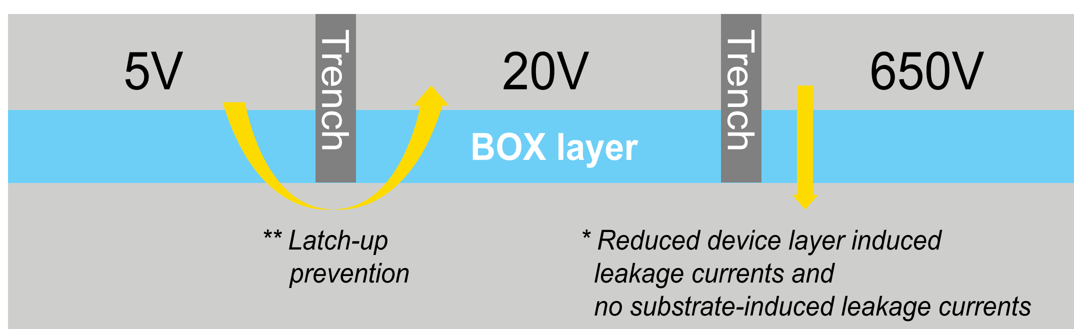
Power GaN Substrate Wafers (Si and SOI)

From standard to extra-thick <111> wafers with advanced stress management for GaN growth. Customized for GaN-on-Si and GaN-on-SOI power device requirements. A highly functional, cost-effective alternative to GaN-on-SiC substrates. Suitable for GaN HEMT devices.

Optimized Power Device Performance

- Volume production for leading power device manufacturers since 1990s.
- Wafers that improve power device performance, reduce Total Cost of Ownership and enable more refined designs.
- Available wafer sizes 150 and 200 mm.

Power Management SOI BOX layer and trench isolation enable reduced chip size with monolithic integration of low, medium and high voltage blocks on the same chip.



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