

## BONDED SOI WAFERS ADD DESIGN FREEDOM AND PERFORMANCE

### B<sup>2</sup>SOI - Bonded SOI

Fully customizable with thick or thin device layer. Also available as Terrace Free version. Suitable e.g. for traditional MEMS devices.

### E-SOI® - Enhanced SOI

Highly uniform wafers with  $\pm 0.1 \mu\text{m}$  thickness variation. Also available as Terrace Free version. Suitable e.g. for silicon photonics and high-precision silicon-based MEMS.

### C-SOI® - Cavity SOI

SOI wafers with embedded / buried cavities. Suitable e.g. for high-precision MEMS.

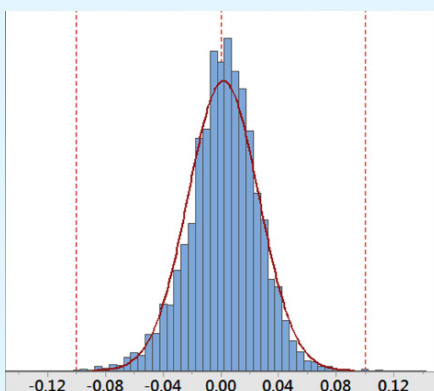
### TSV - Through Silicon Vias

Polysilicon filled TSVs enable isolated electrical connections to be made through silicon wafers.

### Design Freedom, Performance and Ease of Manufacturing

- SOI wafer volume production for leading semiconductor device manufacturers since 2001.
- Device manufacturers benefit from increased design freedom, maximum device performance, cost-effectiveness and ease of manufacturing.
- Customized wafer solutions to meet your device and process needs e.g. possibility for advanced options with two device and BOX layers of different thicknesses.
- Available wafer sizes 150 and 200 mm.
- Fully in-house process covering crystal growth, wafering, SOI bonding, DRIE and lithography.

Device layer thickness capability of E-SOI® wafers



Deviation from target thickness ( $\mu\text{m}$ )

### Typical SOI Wafer Specifications

#### RESISTIVITY

From  $<0.001$  to  $>7,000 \text{ Ohm-cm}$

#### DEVICE LAYER THICKNESS

From  $1 \mu\text{m}$  to  $>200 \mu\text{m}$   
Tolerance  $\pm 0.5 \mu\text{m}$  (standard B<sup>2</sup>SOI),  
 $\pm 0.1 \mu\text{m}$  (200 mm E-SOI®),  $\pm 0.5 \mu\text{m}$  (C-SOI®)

#### HANDLE WAFER THICKNESS

From  $300 \mu\text{m}$  to  $950 \mu\text{m}$ , tolerance  $\pm 3\text{-}5 \mu\text{m}$   
Back surface polished or etched

#### BURIED OXIDE

Type: thermal oxide, thickness from  $0.3 \mu\text{m}$  to  $>5 \mu\text{m}$

